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PATENT

Docket No. SPLX.P0068

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Mani Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 09/972,011

Filing Date: 10/5/2001

For: METHOD AND ARRANGEMENT FOR
LAYOUT AND MANUFACTURE OF
NONMANHATTAN SEMICONDUCTOR
INTEGRATED CIRCUIT USING SIMULATED
EUCLIDEAN WIRING

INFORMATION DISCLOSURE
STATEMENT UNDER 37 C.F.R. § 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to



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Based on PTO/SB/21 (05-03)
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/972,011
	Filing Date	10/5/2001
	First Named Inventor	Steven Teig, et al.
	Group Art Unit	2825
	Examiner Name	Helen Rossoshek
Total Number of Pages in This Submission	Attorney Docket Number	SPLX.P0068

Enclosures (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declarations(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input checked="" type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Documents <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers (for an application) <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosures (Listed below): Postcard 9 cited references Copy of eIDS with a Fee Transmittal
Remarks:		
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm Or Individual name	Mani Adeli, Reg. No. 39,585 of Stattler Johansen & Adeli LLP	
Signature		
Date	July 22, 2004	

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Typed or printed name	Mani Adeli		
Signature		Date	July 22, 2004

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

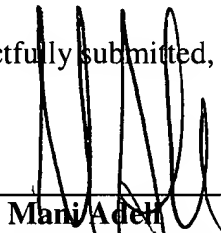
the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is submitted after receipt of a first Office Action on the merits but before the Final Office Action. Accordingly, a fee is required. However, Applicants note that on this day, July 22, 2004, Applicants have submitted another Information Disclosure Statement in electronic form and paid the requisite fee along with this electronic submission. See attached hard copy of electronic IDS and its fee transmittal. Therefore, Applicants submit that no separate fee is required for this Information Disclosure Statement.

However, in the unlikely event that the Patent Office determines that additional fees, extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-1128** referencing SPLX.P0068. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: July 22, 2004

Respectfully submitted,

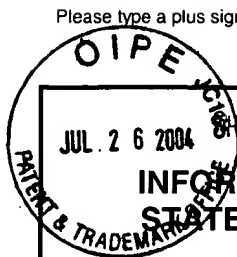
By: 
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Phone No. (650) 752-0990 x102
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Substitute for form 1449A/PTO				Application Number	09/972,011
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	10/5/2001
(use as many sheets as necessary)				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	Helen Rossoshek
				Attorney Docket Number	SPLX.P0068
Sheet	1	of	1		

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FOREIGN PATENT DOCUMENTS

Examiner* Initials	Cite No. ¹	Foreign Patent Document			Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code (if known) ⁵				
	1.	JP	04-000677		01-06-1992	Fujiwara et al.	with English translation of Abstract;	
	2.	JP	2000-082743		03-21-2000	Igarashi et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓

NON PATENT LITERATURE DOCUMENTS

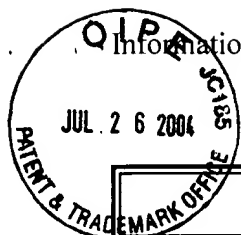
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	3.	Chen et al., Optimal Algorithms for Bubble Sort Based Non-Manhattan Channel Routing, May 1994, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions Volume: 13 Issues, pp. 603-609.	
	4.	Chen, H. et al., Physical Planning of On-Chip Interconnect Architectures, 2002, IEEE, International Conference, pp. 30-35	
	5.	Cong J. et al., DUNE - A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.	
	6.	Dion J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95/3, pp.1-22	
	7.	Merriam-Webster's Collegiate Dictionary, 10 th edition, Merriam-Webster Incorporated, p.606	
	8.	Schiele, W. et al., A Gridless Router for Industrial Design Rule, 27 th ACM-IEEE Design Automation Conference, pp. 626-631, 1990.	
	9.	Tseng H. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.	

Examiner Signature		Date Considered	
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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number(optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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**ELECTRONIC INFORMATION DISCLOSURE STATEMENT**

Electronic Version v18

Stylesheet Version v18.0

RECEIVED**JUL 30 2004****TECH CENTER 2800****Title of
Invention**

Method and arrangement for layout and manufacture of
nonmanhattan semiconductor integrated circuit using
simulated euclidean wiring

Application Number: 09/972011

09/972011

Confirmation Number: 5250

First Named Applicant: Steven Teig

Attorney Docket Number: SPLX.P0068

Art Unit: 2825

Examiner: Helen B. Rossoshek

Search string: (4855253 or 5541005 or 5635736 or 5637920 or
5640327 or 5646830 or 5650653 or 5689433 or
5723908 or 5784289 or 5801385 or 5811863 or
5822214 or 5880969 or 5889329 or 5980093 or
6150193 or 6260183 or 6262487 or 6263475 or
6301686 or 6307256 or 6316838 or 6324674 or
6412097 or 6448591 or 6516455 or 20010009031
or 20030025205).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	4855253	1989-08-08	Weber			
	2	5541005	1996-07-30	Bezama et al.			
	3	5635736	1997-06-03	Funaki et al.			
	4	5637920	1997-06-10	Loo			
	5	5640327	1997-06-17	Ting			
	6	5646830	1997-07-08	Nagano			
	7	5650653	1997-07-22	Rostoker et al.			

	8	5689433	1997-11-18	Edwards	
	9	5723908	1998-03-03	Fuchida et al.	
	10	5784289	1998-07-21	Wang	
	11	5801385	1998-09-01	Endo et al.	
	12	5811863	1998-09-22	Rostoker et al.	
	13	5822214	1998-10-13	Rostoker et al.	
	14	5880969	1999-03-09	Hama et al.	
	15	5889329	1999-03-30	Rostoker et al.	
	16	5980093	1999-11-09	Jones et al.	
	17	6150193	2000-11-21	Glenn	
	18	6260183	2001-07-10	Raspopovic et al.	B1
	19	6262487	2001-07-17	Igarashi et al.	B1
	20	6263475	2001-07-17	Toyonaga et al.	B1
	21	6301686	2001-10-09	Kikuchi et al.	B1
	22	6307256	2001-10-23	Chiang et al.	B1
	23	6316838	2001-11-13	Ozawa et al.	B1
	24	6324674	2001-11-27	Andreev et al.	B2
	25	6412097	2002-06-25	Kikuchi et al.	B1
	26	6448591	2002-09-10	Juengling	B1
	27	6516455	2003-02-04	Teig et al.	B1

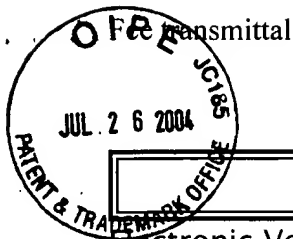
US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20010009031	2001-07-19	Nitta et al.	A1		
	2	20030025205	2003-02-06	Shively	A1		

Signature

Examiner Name	Date



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Electronic Version v08

Stylesheet Version v08.0

TECH CENTER 2800

Title of Invention	Method and arrangement for layout and manufacture of nonmanhattan semiconductor integrated circuit using simulated euclidean wiring										
Application Number: 09/972011 *09/972011*											
Date: 2001-10-05											
First Named Applicant: Steven Teig											
Attorney Docket Number: SPLX.P0068											
Art Unit: 2825											
Examiner: Helen B. Rossoshek											
TOTAL FEE AUTHORIZED \$180											
Patent fees are subject to annual revisions on or about October 1st of each year.											
BASIC FILING FEE											
<table border="1"><thead><tr><th>Fee Description</th><th>Fee Code</th><th>Amount \$</th><th>Fee Paid \$</th></tr></thead><tbody><tr><td>Submission Of Information Disclosure Stmt Fee</td><td>1806</td><td>180</td><td>180</td></tr></tbody></table>				Fee Description	Fee Code	Amount \$	Fee Paid \$	Submission Of Information Disclosure Stmt Fee	1806	180	180
Fee Description	Fee Code	Amount \$	Fee Paid \$								
Submission Of Information Disclosure Stmt Fee	1806	180	180								
AUTHORIZED BILLING INFORMATION											
The commissioner is hereby authorized to charge indicated fees and credit any overpayments to:											
Credit account number: 7556											
Expiration Date (YYYYMMDD): 2004-08-31											
Authorized name: Mani Adeli											
Billing address: 94303											